WHAT IS CLAIMED IS:

1. A method for fabricating a semiconductor device, the method comprising:

providing a semiconductor substrate having a device formation region;

forming a gate on the device formation region of the semiconductor substrate, and forming source and drain regions in the device formation region of the semiconductor substrate adjacent respective sides of the gate, wherein the gate comprises a gate dielectric layer, a gate conductive layer and sidewall spacers located at respective sidewalls of the gate conductive layer;

forming an etch stop layer over the source region, the drain region and the sidewall spacers of the gate to obtain an intermediate structure;

forming a planarized first interlayer insulating film over a surface of the intermediate structure;

dry etching the first insulating layer until the etch stop layer over the source region, the drain region and the sidewall spacers is exposed to form self-aligned contact holes in the first interlayer insulating over the source region and the drain region, respectively;

wet etching the etch stop layer to remove the etch stop layer over the source region, the drain region and the sidewall spacers; and

forming respective contact pads by filling the self-aligned contact holes with conductive polysilicon.

2. The method of claim 1, wherein the gate is formed to further comprise a hard mask on a surface of the gate conductive layer.

3. The method of claim 1, wherein the sidewall spacer and the etch stop layer are formed of silicon nitride by chemical vapor deposition, and the first interlayer insulating film is formed of silicon oxide by chemical vapor deposition.

4. The method of claim 3, wherein the first interlayer insulating film is a silicon oxide film formed by high-density plasma chemical vapor deposition.

5. The method of claim 1, further comprising forming a buffer layer on the source region and the drain region prior to forming the etch stop layer, and removing the buffer layer by wet etching after wet etching the etch stop layer.

6. The method of claim 3, further comprising forming a buffer layer on the source region and the drain region prior to forming the etch stop layer, and removing the buffer layer by wet etching after wet etching the etch stop layer.

7. The method of claim 4, further comprising forming a buffer layer on the source region and the drain region prior to forming the etch stop layer, and removing the buffer layer by wet etching after wet etching the etch stop layer.

8. The method of claim 5, wherein the buffer layer is formed of silicon oxide by thermal oxidation.

9. The method of claim 8, wherein the buffer layer is formed of a mid-temperature oxide (MTO) by low pressure chemical vapor deposition.

10. The method of claim 1, wherein the etch stop layer is formed of silicon nitride by chemical vapor deposition.

11. The method of claim 3, wherein the first interlayer insulating film is formed of silicon oxide by high-density plasma chemical vapor deposition.

12. The method of claim 1, wherein the wet etching of the etch stop layer comprises:

removing oxide film remnants on the etch stop layer by wet etching by with an oxide etchant; and

removing the etch stop layer using an oxide etching solution or a nitride etching solution.

13. The method of claim 12, wherein the oxide etching solution includes hydrofluoric acid (HF) having a density of 0.01 wt% through 0.001 wt%.

14. The method of claim 12, wherein the nitride etching solution includes phosphoric acid H_3PO_4.

15. The method of claim 14, wherein the density of phosphoric acid H_3PO_4 is 50 wt% through 80 wt%.

16. The method of claim 5, wherein the buffer layer is removed using an etching solution including ammonium hydroxide (NH_3OH), hydrogen peroxide (H_2O_2), and deionized water.

17. The method of claim 16, wherein the etching solution includes ammonium hydroxide (NH_3OH) having a density of 0.1 wt% through 1.0 wt%.

18. The method of claim 16, wherein the etching solution includes hydrogen peroxide (H_2O_2) having a density of 4.0 wt% through 7.0 wt%.

19. The method of claim 16, wherein the wet etching is performed at a temperature of 30℃ through 80℃.

20. The method of claim 1, wherein the forming of the respective contact pads comprises:

filling the self-aligned contact holes by depositing the conductive polysilicon over an entirety of the surface of the semiconductor substrate; and

chemical mechanical polishing the conductive polysilicon in the self-aligned contact holes down to a level of an upper portion of the first interlayer insulating film.